IN THE CLAIMS:

Please amend the claims as follows:

1-5. (cancelled)

6. (currently amended) An apparatus for outputting a clock signal for video reconstruction in a terminal, comprising:

an oscillator that generates the clock signal;

a control logic circuit with a phase locked loop for receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal, wherein the control logic circuit outputs a control signal for controlling an output of the oscillator based on the phase lock; and

a frequency range bounder in the phase locked loop that receives the control signal and outputs a bounded control signal that bounds the frequency of the oscillator to a selected range;

wherein the frequency range bounder includes an output multiplexer and a threshold register that stores at least one threshold value and that is coupled to the output multiplexer, wherein the output multiplexer receives a control signal and outputs one of the control signal and said at least one threshold value as a bounded control signal to limit the frequency of the oscillator to the selected range;

wherein said at least one threshold register that stores at least one threshold value is a high limit register that stores an upper value and a low limit register that stores a lower value; and

~~The apparatus of claim 3,~~ wherein the frequency range bounder includes at least one of a minimum function block coupled to the high limit register and a maximum function block coupled to the low limit register, wherein the minimum function block outputs the smaller of the control signal and the upper value and wherein the maximum function block outputs the larger of the control signal and the lower value as the bounded control signal.

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7. (currently amended) An apparatus for outputting a clock signal for video reconstruction in a terminal, comprising:

D1 cont'd

an oscillator that generates the clock signal;

a control logic circuit with a phase locked loop for receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal, wherein the control logic circuit outputs a control signal for controlling an output of the oscillator based on the phase lock; and

a frequency range bounder in the phase locked loop that receives the control signal and outputs a bounded control signal that bounds the frequency of the oscillator to a selected range;

wherein the frequency range bounder includes an output multiplexer and a threshold register that stores at least one threshold value and that is coupled to the output multiplexer, wherein the output multiplexer receives a control signal and outputs one of the control signal and said at least one threshold value as a bounded control signal to limit the frequency of the oscillator to the selected range;

wherein said at least one threshold register that stores at least one threshold value is a high limit register that stores an upper value and a low limit register that stores a lower value; and

~~The apparatus of claim 3,~~ wherein the frequency range bounder includes a comparator coupled to the high limit register and low limit register, wherein the comparator compares the control signal with the upper and lower values and outputs the control signal to the output register if the control signal is between the upper and lower values.

~~8.~~ 3 (original) The apparatus of claim ~~7~~ 2, wherein the frequency range bounder includes an output register coupled to the comparator, and wherein the comparator compares the control signal by comparing data values in the control signal with the upper and lower values and latching the data values in between the upper and lower values into the output register.

9-31. (cancelled).

~~32.~~ 4 (currently amended) A circuit for controlling an oscillator that outputs a clock signal for video reconstruction, comprising:

a control logic circuit with a phase locked loop for receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal, wherein the control logic circuit outputs a control signal for controlling an output of the oscillator based on the phase lock;

a frequency range bounder in the phase locked loop that receives the control signal and outputs a bounded control signal that bounds the frequency of the oscillator to a selected range, wherein said frequency range bounder is configured to generate a high limit signal and a low limit signal and then select one of said control signal, said high limit signal or said low limit signal for transmission to said oscillator depending on whether said control signal remains within pre-defined high and low limits;

~~The circuit of claim 26, further comprising:~~

a minimum function block configured to receive said control signal and said high limit signal, wherein said minimum function block selectively passes whichever signal is lower, said control signal or said high limit signal; and

D1 cont'd

a maximum function block configured to receive an output of said minimum function block and said low limit signal, wherein said maximum function block selectively passes whichever signal is higher, said output from said minimum function block or said low limit signal, to said oscillator.

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~~33~~. (currently amended) A circuit for controlling an oscillator that outputs a clock signal for video reconstruction, comprising:

a control logic circuit with a phase locked loop for receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal, wherein the control logic circuit outputs a control signal for controlling an output of the oscillator based on the phase lock;

a frequency range bounder in the phase locked loop that receives the control signal and outputs a bounded control signal that bounds the frequency of the oscillator to a selected

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range, wherein said frequency range bounder is configured to generate a high limit signal and a low limit signal and then select one of said control signal, said high limit signal or said low limit signal for transmission to said oscillator depending on whether said control signal remains within pre-defined high and low limits;

~~The circuit of claim 26, further comprising:~~

a maximum function block configured to receive said control signal and said low limit signal, wherein said maximum function block selectively passes whichever signal is higher, said control signal or said low limit signal; and

a minimum function block configured to receive an output of said maximum function block and said high limit signal, wherein said minimum function block selectively passes whichever signal is lower, said output from said maximum function block or said high limit signal, to said oscillator.

34-38. (cancelled)

~~29.~~ 6 (currently amended) A method of controlling an oscillator that outputs a clock signal for video reconstruction, wherein said oscillator is controlled to remain within high and low frequency bounds, said method comprising:

receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal;

outputting a control signal for controlling an output of the oscillator based on the phase lock;

generating a high limit signal and a low limit signal;

selecting one of said control signal, said high limit signal or said low limit signal for transmission to said oscillator depending on whether said control signal remains within pre-defined high and low limits;

~~The method of claim 34, further comprising:~~

receiving said control signal and said high limit signal with a minimum function block;

with said minimum function block, selectively passing whichever signal is lower, said control signal or said high limit signal;

receiving an output of said minimum function block and said low limit signal with a maximum function block; and

with said maximum function block, selectively passing whichever signal is higher, said output from said minimum function block or said low limit signal, to said oscillator.

~~40.~~ 41. (currently amended) A method of controlling an oscillator that outputs a clock signal for video reconstruction, wherein said oscillator is controlled to remain within high and low frequency bounds, said method comprising:

receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal;

outputting a control signal for controlling an output of the oscillator based on the phase lock;

generating a high limit signal and a low limit signal;

selecting one of said control signal, said high limit signal or said low limit signal for transmission to said oscillator depending on whether said control signal remains within pre-defined high and low limits;

~~The method of claim 34, further comprising:~~

receiving said control signal and said low limit signal with a maximum function block;

with said maximum function block, selectively passing whichever signal is higher, said control signal or said low limit signal;

receiving an output of said maximum function block and said high limit signal with a minimum function block; and

with said minimum function block, selectively passing whichever signal is lower, said output from said maximum function block or said high limit signal, to said oscillator.

41. (cancelled)